(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 December 2000 (14.12.2000)

PCT

(10) International Publication Number
WO 00/76060 A1

(51) International Patent Classification[7]: H03D 7/16

(21) International Application Number: PCT/US00/15279

(22) International Filing Date: 2 June 2000 (02.06.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/325,100 3 June 1999 (03.06.1999) US

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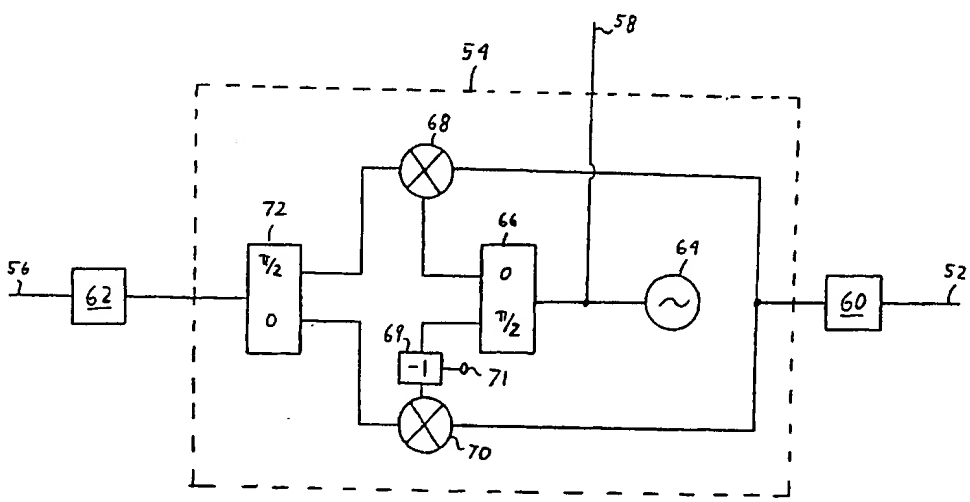
(81) Designated State (national): JP.

(84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

(54) Title: DUAL-BAND IMAGE REJECTION MIXER



(57) Abstract: A rejection converter is disclosed for use in a transmitter for operating in at least either of a first mode for transmitting signals within a first frequency range, and a second mode for transmitting signals within a second frequency range. The rejection converter includes an input unit for receiving an input signal in at least either of the first or second frequency ranges. The rejection converter also includes a rejection unit for rejecting at least one spurious harmonic signal associated with the first frequency range that falls within the second frequency range. The rejection converter permits signals in the second frequency range to be passed when the output signal is within the second frequency range.

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DUAL-BAND IMAGE REJECTION MIXER

BACKGROUND OF THE INVENTION

The invention relates to the field of transmitters for radio frequency communication systems, and particularly relates to transmitters including constant envelope modulation systems.

As wireless communication systems have become increasingly popular, a demand has developed for less expensive yet spectrally clean radio frequency (RF) transmitters having constant envelope modulation systems. High quality RF transmitters typically include relatively expensive components. For example, certain bandpass filters, such as surface acoustic wave (SAW) filters provide excellent performance yet are relatively expensive. Many applications further require transmitters that exhibit low power consumption. It is also desirable that transmitters be suitable for use with any of a plurality of standards for modulation, e.g., global system for mobile communication (GSM) or digital cellular system (DCS).

Constant envelope modulation systems including translation loop modulators are known to provide circuits having relatively less expensive filtering requirements. Translation loop modulators generally include a feedback loop in communication with the output oscillator that is coupled to a transmission antenna. The feedback loop permits the circuit itself to provide bandpass filtering since the output signal may be locked to a given center frequency.

A conventional translation loop modulation system is shown in Figure 1. The system 10 includes quadrature modulation circuitry12, phase comparitor circuitry 14, a voltage controlled oscillator (VCO) 16 coupled to an output antenna (not shown) a feedback coupler 17, and a feedback path 18. Input signals representative of the information to be modulated and transmitted may be applied to the I and Q channels of the quadrature modulator. The input signals may be modulated to adjust the phase or angle of a reference signal. This phase information is converted to a voltage signal by the phase comparitor circuitry 14, and the voltage signal is then converted to a frequency signal by the VCO 16. The feedback path 18 provides a phase locked loop to lock the VCO 16 to a given center frequency.

It is conventionally known that transmitter circuits should be designed to reduce

the possibility of spurious signals (e.g., harmonics as well as foreign signals) being introduced into the system. In certain situations, the origin of some spurious signals may be extremely difficult to discern, particularly if they appear only sporatically, and may be nearly impossible to simulate. To address this problem, it is conventionally believed that transmitter circuits of the type shown in Figure 1 should be designed to be flexible so that they may be adjusted to remove any noise.

For example, in certain situations, a circuit may be most easily corrected by adjusting either the voltage controlled oscillator 20 in the phase comparitor circuitry, or the voltage controlled oscillator 22 in the feedback path. Employing two separate oscillators facilitates adjustment for reducing noise since either may be adjusted independent of the other. Moreover, the frequencies may be chosen so as to not be harmonically related, which minimizes the chance of harmonic spurious signals being produced by the oscillators.

Unfortunately, however, some oscillators are rather expensive. For example, certain oscillator circuits that are formed of synthesizers produce very stable output signals, but are relatively expensive. It is also desirable that the use of relatively expensive filters be avoided.

There is a need, therefore, for inexpensive yet efficient constant envelope modulation systems for use with dual mode transmitters. There is further a need for a translation loop modulator that is spectrally efficient yet economical to produce.

SUMMARY OF THE INVENTION

The invention provides a rejection converter for use in a transmitter, such as a translation loop modulator, for operating in at least either of a first mode for transmitting signals within a first frequency range, and a second mode for transmitting signals within a second frequency range. The converter includes an input unit for receiving an input signal in at least either of the first or second frequency ranges. The converter also includes a rejection unit for rejecting at least one spurious harmonic signal associated with the first frequency range that falls within the second frequency range. The converter permits signals in the second frequency range to be passed when the output signal is within the second frequency range.

BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description may be further understood with reference to the accompanying drawings in which:

FIG. 1 shows a functional block diagram of a conventional translation loop modulator;

FIG. 2 shows a functional block diagram of a translation loop modulator including an image rejection downconverter of an embodiment of the invention; and

FIG 3 shows a functional block diagram of the image rejection downconver shown in FIG 2.

DETAILED DESCRIPTION OF THE INVENTION

It has been discovered that a translation loop modulator may include a reference oscillator that provides a local oscillator signal to both the phase comparator circuitry and to the feedback path. As shown in Figure 2, a system 30 of an embodiment of the invention includes quadrature mixer circuitry including two mixers 32 and 34, a phase shift device 36, a summing device 38 and a bandpass filter 40. One input signal to the first mixer 32 is the *I* channel (or In Phase channel) input modulation signal, and the other is a feedback signal 56 without a phase shift. The output of the mixer 32 is coupled to the summing device 38. One input signal to the second mixer 34 is the *Q* channel (or Quadrature channel) input modulation signal, and the other is a phase shifted feedback signal that is produced by the phase shift device 36. In other embodiments, various combinations of phase shifting may be employed to achieve quadrature modulation of the input signals. The output of the mixer 34 is combined with the output of the mixer 32 at the summing device 38 to produce a combined signal. This combined signal is filtered by bandpass filter 40 to produce a quadrature modulation signal.

The phase comparitor circuitry of the embodiment shown in Figure 2 includes an *m* frequency divider 42, a phase comparitor device 44, an *n* frequency divider 46, and a loop filter 48. The quadrature modulation signal is input to the *m* frequency divider 42. The phase comparitor device receives one input from the output of the *m* frequency divider 42, and the other input from the *n* frequency divider 46. The output of the phase comparitor device 44 is coupled to a bandpass filter 48, the output of which is coupled to an output VCO 50. The VCO 50 produces the transmitter output signal 52, and is coupled to a power amplifier (not shown) as well as an antenna (not shown).

Downconverter circuitry 54 is provided together with low pass filter 60 and

bandpass filter 62 in the feedback path to translate the frequency of the output signal 52 RF_{OUT} to an intermediate frequency RF_{IF} (the frequency of the feedback signal 56). The downconverter circuitry 54 is provided a reference signal 58 at a local oscillator frequency RF_{LO}, and this reference signal is provided to the n frequency divider 46 of the phase comparator circuitry. One VCO only may, therefore, provide an oscillator signal to both the phase comparitor circuitry and to the downconverter mixer in the feedback circuitry. This is achieved through careful selection of components and frequency plan.

Each mixer will produce signals having frequencies at the sum as well as at the difference between the frequencies of the two input signals. In particular, the product of two sine functions $\sin(\alpha) \times \sin(\beta)$ equals $\frac{1}{2}\cos(\alpha-\beta) - \frac{1}{2}\cos(\alpha+\beta)$. The two frequencies produced at the output, therefore, would be F_1+F_2 and $F_1 - F_2$. One of the two signal frequencies may then be filtered out. The quadrature modulation signal is then coupled to phase comparator circuitry.

The circuit provides that the frequency of the transmitter output signal (RF_{OUT}) may be related to the frequency of the local oscillator signal (RF_{LO}) in either of two ways, either $RF_{LO}/n = (RF_{LO} - RF_{OUT})/m$, or $RF_{LO}/n = (RF_{LO} + RF_{OUT})/m$. The first relationship provides that $RF_{LO} = RF_{OUT} \times n / (n-m)$ and the second relationship provides that $RF_{LO} = RF_{OUT} \times n / (n+m)$. The values of m and n may be chosen such that the transmitter output signal may be at 900 MHz for GSM, and may be at 1800 MHz for DCS. This may be achieved by recognizing that $RF_{OUT} = RF_{LO} + RF_{IF}$ for DCS and $RF_{OUT} = RF_{LO} - RF_{IF}$ for GSM where RF_{IF} is the frequency of the intermediate frequency signal, which is the feedback signal to the quadrature modulator.

During operation, the output of the phase comparitor 44 provides a dc voltage responsive to the phase difference between two input signals of the same frequency. For example. the input signals to the phase comparitor 44 may each be 225 MHz in frequency. If $m=2$ and $n=6$, then the signal input to the m frequency divider 42 must be 450 MHz in frequency, and the signal input to the n frequency divider 46 must be 1350 MHz. For GSM, the output signal produced by the transmit oscillator will be 900 MHz in frequency. This signal is output to the transmitter antenna (not shown). For these values of m and n, therefore, $RF_{LO} = 3/2\ RF_{OUT}$ for GSM, $RF_{LO} = 3/4\ RF_{OUT}$ for DCS.

By controlling I and Q, the phase (or angle) of the 450 MHz signal that is input to the m divider 42 may be precisely controlled. For example, if zero volts is applied on the Q input and one volt is applied to the I input, then the signal provided to the divider

circuitry would be a 450 MHz signal at zero degrees. If zero volts is applied on the Q input and negative one volt on the I input, then the quadrature output signal would be a 450 MHz signal at 180 degrees. If one volt is applied on the Q input and zero volts on I input, then the output signal would be a 450 MHz signal at 90 degrees. If negative one volt is applied on the Q input and zero volts is applied to the I input, then the output signal would be a 450 MHz signal at -90 degrees. By adjusting the I and Q inputs, the angle of the 450 MHz signal may be fully adjusted.

The quadrature modulator therefore provides the modulation for the RF output signal. The output of the phase comparitor produces a signal at the frequency of the sum of the inputs, as well as a signal at a frequency of the difference between the inputs. The signal at the sum frequency (450 MHz) is filtered out at the filter 48, and the dc signal (zero MHz.) is input to the voltage controlled oscillator, which in turn, produces the output signal for the antenna. The filter 48 also filters any other noise that may develop in the system. The output of divider 46 is not modulated, whereas the output of divider 42 is modulated. The output of device 44 and filter 48 is a DC voltage including modulation information.

With proper selection of the downconverter oscillator, the filters 40 and 48, and the values of the frequency dividers 42 and 46, a translation loop modulator circuit may be provided using one oscillator that is coupled to the phase comparator circuitry and the feedback circuitry. In other embodiments, the values of m and n may be different, e.g, $m = 2$ and $n = 6$. In this case as well, however, $RF_{LO} = 3/2\ RF_{OUT}$ for GSM, and $RF_{LO} = ¾\ RF_{OUT}$ for DCS.

Higher order intermodulation products may be low pass filtered, but the image frequency must be filtered or rejected. Since $RF_{IF} = (m/n)\ RF_{LO}$, the frequency of the output signal RF_{OUT} may be described as $RF_{OUT} = RF_{LO}\ (1+m/n)$ for DCS and $RF_{OUT} = RF_{LO}\ (1-m/n)$ for GSM. The translation, therefore, of the frequency of the output signal RF_{OUT} to the intermediate frequency RF_{IF} may be described as $RF_{IF} = |K \times RF_{OUT} - J \times RF_{LO}|$, where K and J are integers. In a distortion-less system, K=J=1. In a system exhibiting some distortion, J and K represent the harmonic orders of both RF_{LO} and RF_{OUT} respectively, which may also create products at RF_{IF}. These harmonics may be generated by the transmit VCO 50, the reference oscillator, or by non-linearities in the downconverter circuitry. Since J represents the harmonic value of RF_{LO}, and K represents the harmonic value of RF_{OUT}, the values of J and K may be determined from the

relationship $J = K + (K \pm 1)(m/n)$ for DCS and $J = K - (K \pm 1)(m/n)$ for GSM, again, where J, K, m and n are integers.

For example, in a GSM system where $m = 2$ and $n = 6$, $K = 2$ (the second harmonic of the transmit VCO) and $J = 1$ (the fundamental of the reference oscillator). For a dual mode radio, the second harmonic of the GSM transmit output signal falls into the DCS transmit band, and cannot be simply filtered. For this choice of m and n, $RF_{OUT} = 2RF_{IF}$ since $RF_{OUT} = RF_{LO} - RF_{IF} = 6/2\ RF_{IF} - RF_{IF}$. The second harmonic of the GSM frequency is the image frequency of the desired response. An image rejection mixer may be used to accommodate both GSM and DCS modes.

The circuit may include two separate VCOs with transmit filters to provide the necessary filtering, but such a circuit adds costs and complexity to the circuit, and further may add distortion. A switched filter may also provide the required filtering, but such filters also add cost and complexity to the circuit, and also may add distortion.

As shown in FIG. 3, the downconverter circuitry 54 of the embodiment shown in FIG. 2 includes a VCO 64 that is coupled to the n frequency divider 46 (shown in FIG. 2) and a quadrature divider 66. The VCO 64 produces the local oscillator signal 58. The quadrature divider 66 is coupled to two mixers 68 and 70, each of which is also coupled to the low pass filter 60 in communication with the output transmit signal. The quadrature divider 66 produces two signals, one having a phase shift of 90 degrees and the other with zero degrees phase shift. The zero degree phase shift signal from the quadrature divider 66 is input to the first mixer 68, and the 90 degree phase shift signal from the quadrature divider 66 is coupled to the second mixer 70 via a selective inverter 69. The output of the low pass filter 60 is also input to each of the mixers 68 and 70. The selective inverter 69 selectively inverts an input signal responsive to a selection signal at 71. In GSM mode the selective inverter is disabled and therefore does not invert the input signal thereof, and in DCS mode the selective inverter is enabled by applying an enable signal at 71.

The output of the first mixer 68 is coupled to a 90 degrees phase shift input of a quadrature combiner 72,and the output of the second mixer 70 is coupled to a zero degrees phase shift input of the quadrature combiner 72. The output of the quadrature combiner is coupled to the bandpass filter 62, which in turn, is coupled to the quadrature modulation circuitry shown in FIG.2.

The operation of the circuit may be further described with reference to FIG.3, as well as a discussion of the relationships between the signals. In short, the described

circuit provides that signals at the GSM frequency are passed, as are signals at the DCS frequency, but signals at twice the GSM frequency are rejected.

For GSM operation, $RF_{OUT} = RF_{LO} - RF_{IF}$, which may be written as $\omega_G = \omega_L - \omega_I$. This represents the difference product. The feedback signal (a_1) from the low pass filter 60 may be represented as $\sin(\omega_L - \omega_I)t = \sin \omega_G t$. The signal ($a_2$) produced by the VCO 64 and passed through the quadrature divider 66 (at zero phase) to the mixer 68 may be represented as:

$a_2 = \sin \omega_L t$, and the phase shifted signal that is coupled to the other mixer is:

$$a_2' = \sin(\omega_L t + \pi/2) = \cos \omega_L t.$$

The signal (a_3) produced by the mixer 68 is given by

$$a_3 = \sin(\omega_L - \omega_I)t \times \sin \omega_L t = ½ \cos(\omega_L - \omega_I - \omega_L)t - ½ \cos(\omega_L - \omega_I + \omega_L)t; \text{ or}$$

$$a_3 = ½ \cos(-\omega_I)t - ½ \cos(2\omega_L - \omega_I)t$$

The second term is ultimately filtered by filter 62, so it can be ignored here. Since $\cos(-\alpha) = \cos \alpha$, a_3 may be expressed as:

$$a_3 = ½ \cos \omega_I t$$

The signal (a_4) that is produced by the mixer 70 is provided by:

$$\begin{aligned} a_4 = a_1 a_2' &= \sin(\omega_L - \omega_I)t \times \sin(\omega_L t + \pi/2) \\ &= \sin(\omega_L - \omega_I)t \times \cos \omega_L t \\ &= ½ \sin(2\omega_L - \omega_I)t + ½ \sin(-\omega_I)t \\ &= ½ \sin(2\omega_L - \omega_I)t + ½ \sin(-\omega_I)t \end{aligned}$$

The first term is rejected by filter 62, so it can be ignored. Since $\sin(-\alpha) = -\sin \alpha$, then a_4 may be expressed as $a_4 = -½ \sin \omega_I t$.

The output signal a_0 may be expressed as $a_3' + a_4$, where

$$a_3' = ½ \cos(\omega_I t + \pi/2) = -½ \sin \omega_I t.$$

So, $a_0 = -\frac{1}{2}\sin\omega_I t + (-\frac{1}{2}\sin\omega_I t) = -\sin\omega_I t$.

The undesired GSM harmonic is filtered as follows. The sum product $\omega_L + \omega_I = 2\omega_G$. In this case,

$$a_1 = \sin(\omega_L + \omega_I)t = \sin 2\omega_G t$$

$$a_2 = \sin\omega_L t, \text{ and}$$

$$a_3 = a_1 a_2 = \sin(\omega_L + \omega_I)t \times \sin\omega_L t$$

$$= \tfrac{1}{2}\cos(\omega_L - \omega_I - \omega_L)t - \tfrac{1}{2}\cos(\omega_L + \omega_I + \omega_L)t$$

$$= \tfrac{1}{2}\cos\omega_I t - \tfrac{1}{2}\cos(2\omega_L + \omega_I)t$$

Again, the second term is filtered by the filter 62, so $a_3 = \frac{1}{2}\cos\omega_I t$. The phase shifted term (a_3') is expressed as,

$$a_3' = \tfrac{1}{2}\cos(\omega_I t + \pi/2) = -\tfrac{1}{2}\sin\omega_I t$$

Since $a_4 = a_1 a_2'$,

$$a_4 = \sin(\omega_L + \omega_I)t \times \sin(\omega_L t + \pi/2)$$

$$= \sin(\omega_L + \omega_I)t \times \cos\omega_L t$$

$$= \tfrac{1}{2}\sin(\omega_L + \omega_I + \omega_L)t + \tfrac{1}{2}\sin(\omega_L + \omega_I - \omega_L)t$$

$$= \tfrac{1}{2}\sin(2\omega_L + \omega_I)t + \tfrac{1}{2}\sin\omega_I t$$

Again, the first term is rejected by filter 62, so it can be ignored. The signal (a_4) may therefore be expressed as $a_4 = \frac{1}{2}\sin\omega_I t$.

In this case, the output signal a_0 may be expressed as $a_3' + a_4$, where

$$a_3' = \tfrac{1}{2}\cos(\omega_I t + \pi/2) = -\tfrac{1}{2}\sin\omega_I t.$$

$$\text{So, } a_0 = -\tfrac{1}{2}\sin\omega_I t + \tfrac{1}{2}\sin\omega_I t = o.$$

For DCS, the signal (a_2) must be inverted prior to being input to the mixer 70. The signal a2 is inverted by the selective inverter 69 that inverts an input signal responsive to a selector signal at 71. In GSM mode, the selector signal does not direct the selective inverter 69 to invert the input signal. In DCS mode, the selector signal is enabled causing the selective inverter 69 to invert its input signal (a_2) and produce an inverted signal ($-a_2$)

which is input to the mixer 70 as shown in Figure 3.

Solving for the signal (a_1) entering mixers 68 and 70 from the filter 60, $a_1 = \sin(\omega_L + \omega_I)\, t = \sin \omega_D\, t$. The signal produced by the VCO 64 (a_2) is given by

$$a_2 = \sin \omega_L, \text{ and}$$

$$a_2' = \sin(\omega_L t + \pi/2) = \cos \omega_L t.$$

The signal produced by the mixer 68 (a_3) is given by $a_3 = a_1 a_2$, or

$$\begin{aligned} a_3 &= \sin(\omega_L + \omega_I)\, t \text{ x } \sin \omega_L t \\ &= \tfrac{1}{2} \cos(\omega_L + \omega_I - \omega_L)\, t - \tfrac{1}{2} \cos(\omega_L + \omega_I + \omega_L)\, t \\ &= \tfrac{1}{2} \cos \omega_I t - \tfrac{1}{2} \cos(2\omega_L + \omega_I)\, t \end{aligned}$$

Again, the second term is filtered, so $a_3 = \tfrac{1}{2} \cos \omega_I t$. The signal a_3' produced internally by the quadrature divider 66 responsive to a_3 is provided by:

$$a_3' = \tfrac{1}{2} \cos(\omega_I t + \pi/2) = -\tfrac{1}{2} \sin \omega_I t.$$

The signal a_4 produced by the mixer 70 is given by $a_4 = a_1 \text{ x } (-a_2')$, or

$$\begin{aligned} a_4 &= \sin(\omega_L + \omega_I)\, t \text{ x } -\sin(\omega_L t + \pi/2) \\ &= -\sin(\omega_L + \omega_I) t \text{ x } \cos \omega_L t \\ &= -\tfrac{1}{2} \sin(\omega_L + \omega_I + \omega_L)\, t - \tfrac{1}{2} \sin(\omega_L + \omega_I - \omega_L)\, t \\ &= \tfrac{1}{2} \sin(2\omega_L + \omega_I) t - \tfrac{1}{2} \sin \omega_I t. \end{aligned}$$

Since the first term is filtered, $a_4 = -\tfrac{1}{2} \sin \omega_I t$

Solving, therefore, for the feedback signal (a_0) for DCS provides that:

$$a_0 = a3' + a4, \text{ or}$$

$$a_0 = -\tfrac{1}{2} \cos \omega_I t + \tfrac{1}{2} \cos \omega_I t, \text{ or}$$

$$a_0 = -\sin \omega_I t.$$

The product, therefore, resulting from twice the signal for GSM is rejected while the fundamental GSM signal (x1) is passed. By inverting the signal a_2', DCS mode is

accommodated with a minimum amount of additional circuitry.

Those skilled in the art will appreciate that numerous modifications and variations may be made to the above disclosed embodiments without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A rejection converter for use in a transmitter for operating in at least either of a first mode for transmitting signals within a first frequency range, and a second mode for transmitting signals within a second frequency range, said rejection converter comprising:

input means for receiving an input signal in at least either of said first or second frequency ranges; and

rejection means for rejecting at least one spurious harmonic signal associated with said first frequency range that falls within said second frequency range, and for permitting signals in said second frequency range to be passed when said output signal is within said second frequency range.

2. A rejection converter as claimed in claim 1, wherein transmitter is a translation loop modulator and said rejection converter forms a portion of a feedback path of the translation loop modulator.

3. A rejection converter as claimed in claim 1, wherein said input means for said rejection converter is coupled to the output transmission signal of the transmitter.

4. A rejection converter as claimed in claim 1, wherein said transmitter is a translation loop modulator comprising phase comparator circuitry, and said rejection converter is coupled to said phase comparator circuitry to provide a reference signal to the phase comparator circuitry.

5. A rejection converter as claimed in claim 1, wherein said transmitter is a translation loop modulator comprising a feedback path and a quadrature modulator, and said rejection converter is coupled to the quadrature modulator.

6. A rejection converter as claimed in claim 1, wherein said rejection converter further includes oscillator means for generating a reference signal.

7. A rejection converter as claimed in claim 1, wherein said rejection converter further includes quadrature components for quadrature dividing a reference signal.

8. A rejection converter as claimed in claim 1, wherein said rejection converter further includes quadrature components for quadrature combining at least two component signals.

9. A mixer unit as claimed in claim 1, wherein said mixer unit further includes a pair of mixers, each of said pair of mixers for combining the input signal with a quadrature phase shifted reference signal.

10. A downconverter for use in a translation loop modulator for outputing transmission signals in at least either of a first or second frequency range, said downconverter comprising:

input means for receiving output transmission signals in at least either of said first or second frequency range;

oscillator means for generating a reference signal; and

quadrature rejection means for rejecting a spurious harmonic signal having a frequency that is an integer multiple of an input signal that is within said first frequency range, wherein said spurious harmonic signal is within said second frequency range, and wherein said quadrature rejection means permits output transmission signals within said second frequency range to be passed through said downconverter.

11. A downconverter as claimed in claim 10, wherein said downconverter further includes quadrature components for quadrature dividing the reference signal.

12. A downconverter as claimed in claim 10, wherein said downconverter further includes quadrature components for quadrature combining at least two component signals.

13. A downconverter as claimed in claim 10, wherein said downconverter further includes a pair of mixers, each of said pair of mixers for combining the input signal with a quadrature phase shifted reference signal.

14. A translation loop modulator for outputing transmission signals in either of a first or second frequency range, said translation loop modulator comprising:

input modulation means for receiving at least one input signal that is representative

of information to be modulated, for receiving a feedback signal, and for producing an intermediate modulated signal responsive to said input signal and said feedback signal;

comparator means for receiving said intermediate modulated signal and a reference signal, and for producing an output transmission signal responsive to said intermediate modulated signal and said reference signal;

image rejection feedback circuitry coupled to said output transmission signal, and to said input modulation means, said feedback circuitry including rejection means for rejecting a spurious harmonic signal having a frequency that is an integer multiple of an output transmission signal that is within said first frequency range, wherein said spurious harmonic signal is within said second frequency range, and wherein said image rejection feedback circuitry permits output transmission signals within said second frequency range to be passed through said image rejection feedback circuitry.

15. A translation loop modulator as claimed in claim 14, wherein said image rejection feedback circuitry includes oscillator means for generating a reference signal.

16. A translation loop modulator as claimed in claim 14, wherein said image rejection feedback circuitry includes quadrature divider means for quadrature dividing a reference signal.

17. A translation loop modulator as claimed in claim 14, wherein said image rejection feedback circuitry includes quadrature combiner means for combining at least two quadrature related signals that have been mixed with the output transmission signal.

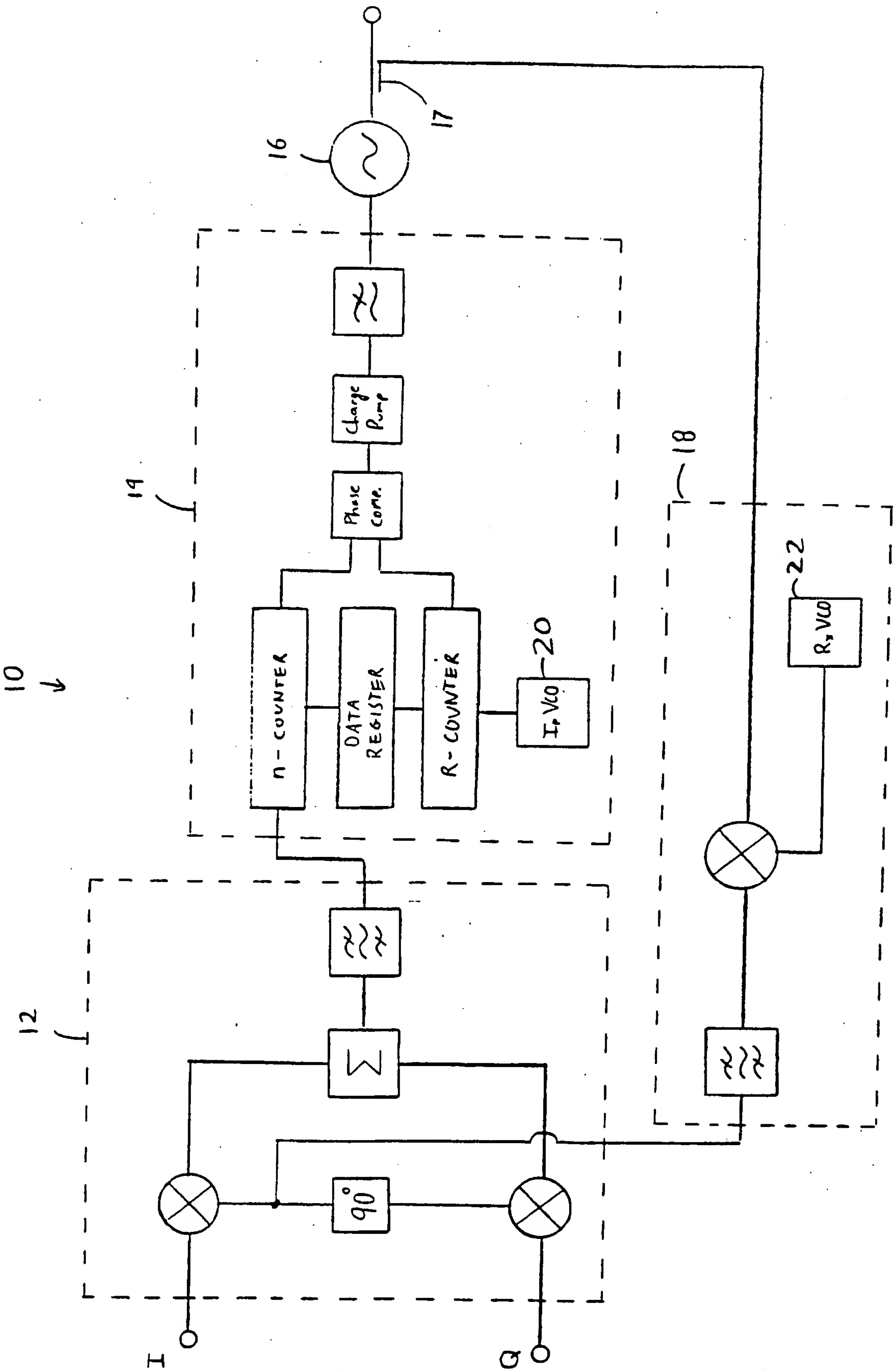

FIG. 1 (PRIOR ART)

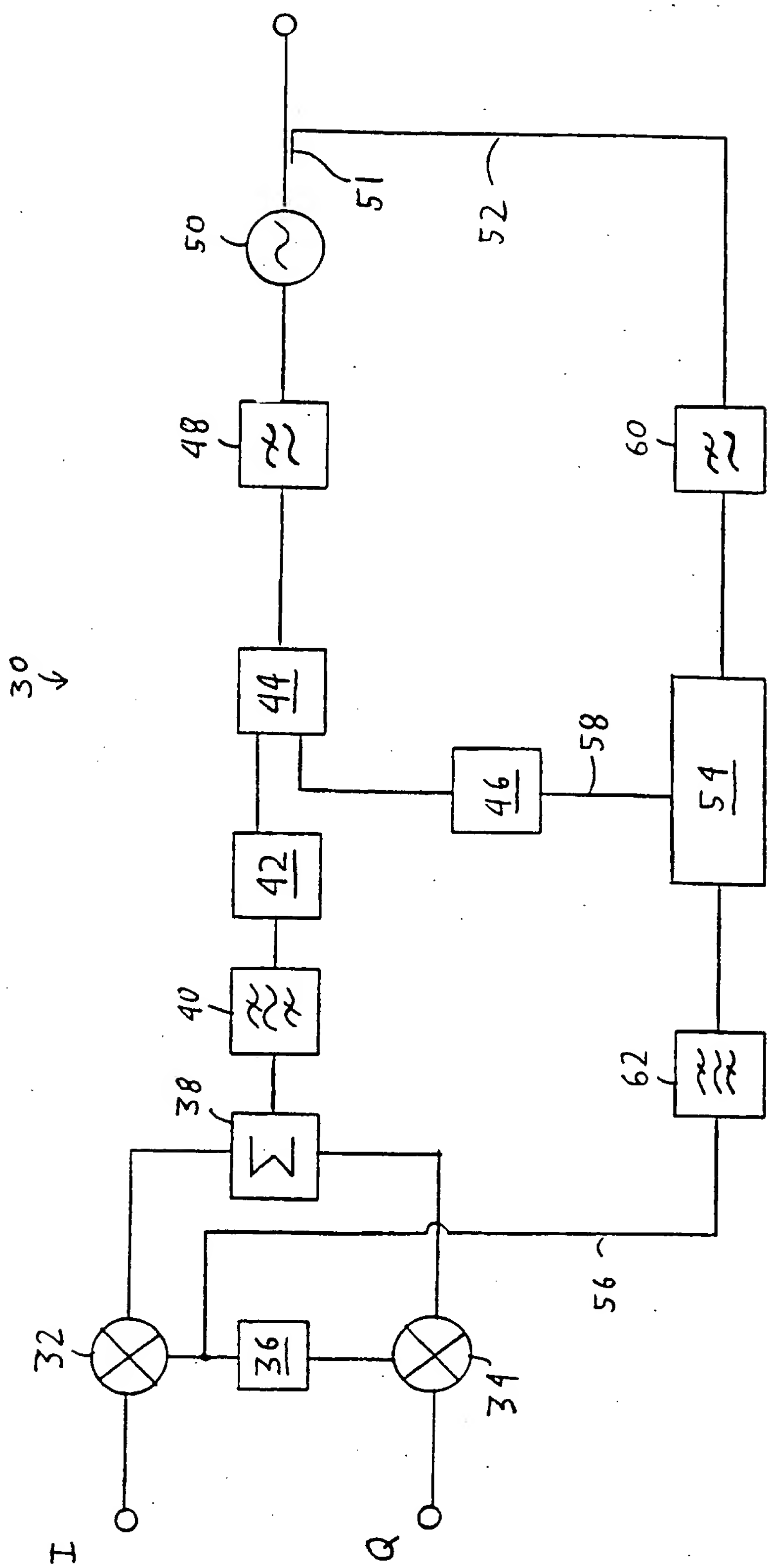

FIG. 2

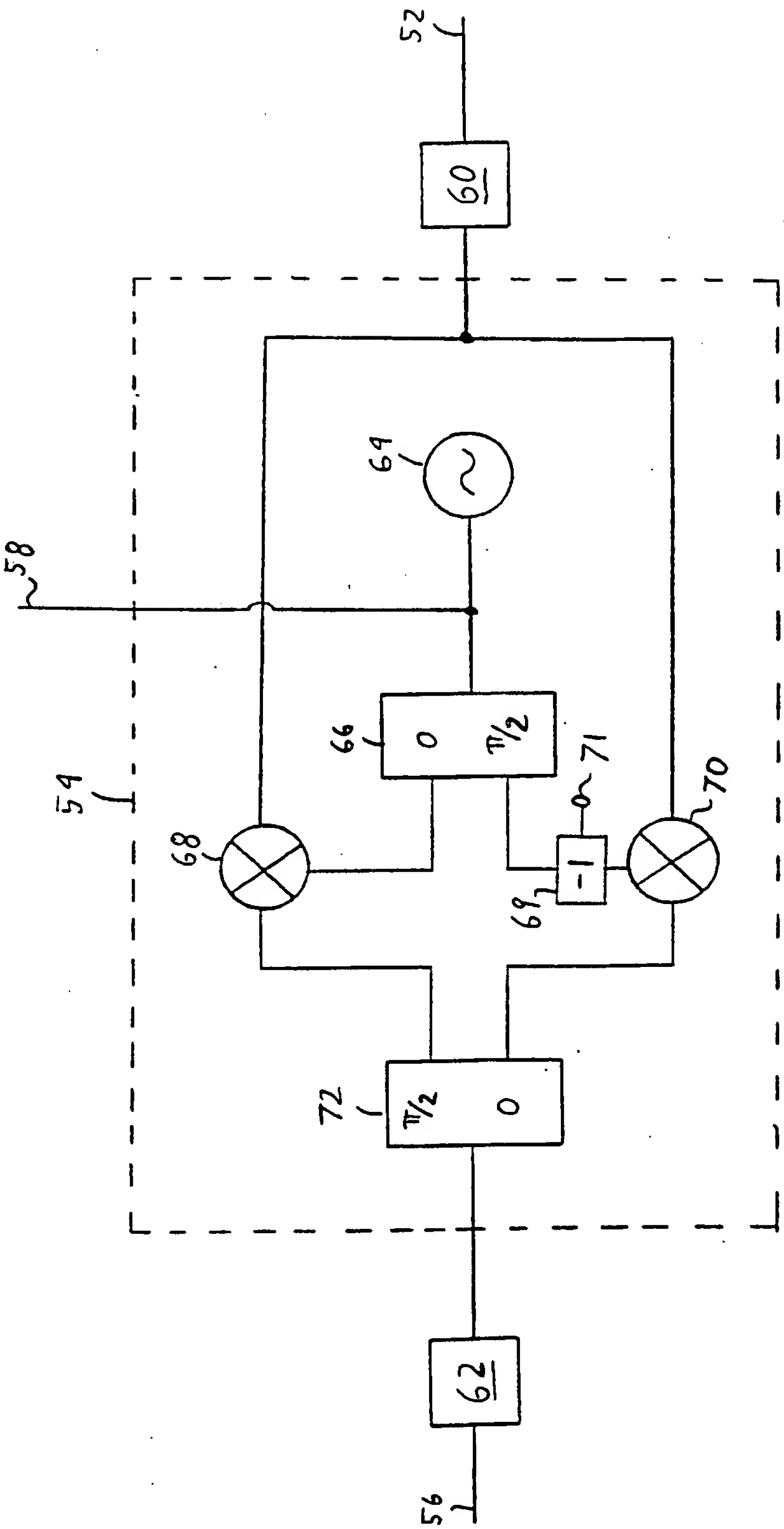

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/15279

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03C H04L H04B H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

WPI Data, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 296 613 A (UNIVERSITY OF BRISTOL) 3 July 1996 (1996-07-03) page 3, line 2 - line 17 column 1, line 20 - line 29; figure 1 page 6, line 13 -page 8, line 35; figure 2 ---	1,3,6-13
X	EP 0 739 090 A (NOKIA MOBILE PHONES LTD) 23 October 1996 (1996-10-23) column 5, line 34 -column 11, line 2; figures 4-7 column 3, line 11 - line 27 page 1, line 23 -page 2, line 2; figure 4 page 3, line 11 -page 4, line 15; figure 6 ---	1,3,6-13
X	US 5 410 743 A (W. SEELY) 25 April 1995 (1995-04-25) column 5, line 24 -column 6, line 54; figures 1-4 --- -/--	1,3,6-13

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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9 October 2000	16/10/2000

Name and mailing address of the ISA	Authorized officer
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